REMARKS

Claims 1-22 will be pending upon entry of the present amendment. Claims 1, 12, and 15 are being amended. Claims 23-25 were previously canceled. No new matter is being presented.

One embodiment of the present invention provides an electronic device for the recording/reproduction of voice data that is entirely integrated in a chip of semiconductor material. It should be emphasized that the components of the electronic device, including the main transmission line; control unit; signal-conversion unit; non-volatile memory unit, and memory controller, are *all integrated in the same chip*. The advantages of this single-chip integration include a smaller device size and reduced power consumption. In addition, the unique architecture of the single-chip integration enables the device to optimize editing of the voice messages itself.

Claims 1-3 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,453,281 to Walters et al. ("Walters") in view of U.S. Patent No. 6,145,060 to Takasu et al. ("Takasu").

Walters and Takasu do not teach or suggest the invention recited in claim 1, as amended. Claim 1 recites "An electronic device for the recording/reproduction of voice data, comprising: a chip of semiconductor material; a main transmission line integrated in said chip; a control unit integrated in said chip…; a signal-conversion unit integrated in said chip; a non-volatile memory unit integrated in said chip…; and a memory unit interface integrated in said chip and coupled between the non-volatile memory unit and said main transmission line, the memory unit interface being structured to coordinate exchange of data and instructions between the non-volatile memory unit and said main transmission line" (Underlined material is being added)[1]. Further, amended claim 1 recites that the control unit is structured to provide a user interface to a user via an external user interface device[2].

Walters and Takasu do not teach or suggest a such a control unit and a memory unit interface *integrated in the same chip of semiconductor material*. Walters does not suggest integrating any two devices (such as those in Figure 4) into a single chip of semiconductor

[1] Support can be found in the paragraph beginning at page 4, line 22.
[2] Support can be found in the paragraph beginning at page 4, line 1.

material. Takasu does not provide the missing teaching because Takasu explicitly shows a control unit 7, which provides a user interface via external devices 3 and 14, on a first chip 1 and a memory controller 22 and memory 25 on a second chip. Further, Takasu explicitly teaches away from incorporating the control unit 7 on the same chip as the memory controller 22 and memory 25. Takasu states at col. 1, lines 38-46:

> Such a nonvolatile memory, however, requires a very high driving voltage, as compared with a CMOS circuit that operates on about 1V, for example. For this reason, an electronic circuit for controlling recording and reproducing operations or image data storing and reading operations that operates on a relatively low voltage and an electronic circuit including nonvolatile memories *have to be composed on separate chips*, which need to being controlled by different voltages separately.

Takasu does not provide any suggestion of a desire to, or of how to, overcome such an explicit statement that the control circuit and nonvolatile memory circuit have to be composed on separate chips. Instead, Takasu confirms that the control integrated circuit 1, which includes the control unit 7, and the memory integrated circuit 2, which includes the memory controller 22 and memory 25, operate on different driving voltages (col. 2, line 67 – col. 3, line 20). Thus, Takasu does not provide any reason to suspect that one could incorporate a control unit structure to provide a user interface on the same chip as a memory unit interface and a memory.

For the foregoing reasons, claim 1 is nonobvious in view of Walters and Takasu.

Claims 2-3 depend on claim 1, and thus, also are nonobvious in view of Walters and Takasu.

Claims 4-5, 12-13, and 15-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters and Takasu in view of Unno et al., EP 0 851 423 A1 ("Unno").

The cited references do not teach or suggest the invention recited in claims 4 and 5, which depend on claim 1. Unno does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because Walters and Takasu do not include all of the recited elements of claim 1, modifying Walters and Takasu by incorporating the teachings of Unno (a buffer memory) would not satisfy the limitations of claims 4 and 5. Accordingly, claims 4-5 are nonobvious in view of the cited prior art.

Although the language of claims 12-13 and 15-16 is not identical to that of claims 4-5, the nonobviousness of claims 12-13 will be apparent in view of the above discussion.

Claims 6 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters, Takasu, and Unno in view of U.S. Patent No. 5,787,445 to Daberko.

The cited prior art references do not teach or suggest the invention recited in claims 6 and 7, which depend from claim 1. Daberko does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Walters, Takasu, and Unno do not include all of the recited elements of claim 1, modifying those teachings by incorporating the teachings of Daberko (first and second cache memories) would not satisfy the limitations of claims 6 and 7. Accordingly, claims 6-7 are nonobvious in view of the cited prior art.

Claims 8, 14, and 17-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters, Takasu, and Unno in view of U.S. Patent No. 6,016,522 to Rossum.

The cited prior art references do not teach or suggest the invention recited in claim 8, which depends from claim 1. Rossum does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Walters, Takasu, and Unno do not include all of the recited elements of claim 1, modifying those teachings by incorporating the teachings of Rossum ("ping-pong" buffering) would not satisfy the limitations of claim 8. Accordingly, claim 8 is nonobvious in view of the cited prior art.

Although the language of claim 14 and 17-19 is not identical to that of claim 8, the nonobviousness of claims 14 and 17-19 will be apparent in view of the above discussion.

Claims 9-11 and 20-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Walters and Takasu in view of U.S. Patent No. 6,604,168 to Ogawa.

Walters, Takasu, and Ogawa do not teach or suggest the invention recited in claims 9-11. Ogawa does not disclose anything about a single-chip integrated electronic device as recited in claim 1. Therefore, because the teachings of Walters and Takasu does not include all of the recited elements of claim 1, modifying those teachings by incorporating the teachings of Ogawa (flash EEPROM management system) would not satisfy the limitations of claims 9-11. Accordingly, claims 9-11 are nonobvious in view of the cited prior art.

Claims 20-22 were rejected under 35 U.S.C. § 103 as being unpatentable over Walters, Takasu, and Unno in view of Ogawa. As discussed above Unno and Ogawa do not teach anything about a single-chip integrated electronic device as recited in claim 15, from which claims 20-22 depend. Accordingly, claims 20-22 are nonobvious in view of the cited prior art.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/Robert Iannucci/
Robert Iannucci
Registration No. 33,514

RXI:vsj

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104-7092
Phone: (206) 622-4900 / Fax: (206) 682-6031
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